What is claimed is:

1. A comparator outputting one bit digital signal after comparing two analog input signals by alternately performing a track mode operation and latch mode operation decided according to a clock signal having a constant period, the comparator comprising:

a differential input unit inputting the two analog input signals, wherein the two analog input signals are treated as a different input;

a tracking/latching unit respectively performing a tracking and latching operation through receiving a differential output of the differential input unit from an ordinary/sub input terminal and having a different current pass from each of the ordinary/sub input terminal of the tracking/latching unit itself in order to make the tracking/latching unit itself operated as a load of the differential input unit for a tracking operation in the track mode; and

a latching unit latching and outputting an output of the tracking/latching unit.

2. The comparator as recited in claim 1, wherein the tracking/latching unit includes:

a latching unit having the main/sub input terminal;

a first switching transistor having the clock signal as a gate input and having one end coupled to main input

terminal;

a first load transistor diode-connected to the other end of the first switching transistor and a ground end;

a second switching transistor having a gate receiving the clock signal as a gate input and one end coupled to the sub input terminal; and

a second load transistor diode-connected to the second switching transistor and to the other end of the ground terminal.

3. The comparator as recited in claim 2, wherein the first load transistor and the second load transistor are large enough to neglect the first switching transistor and the second switching transistor, respectively.

4. The comparator as recited in claim 3, wherein size of the first switching transistor is identical to that of the second switching transistor and size of the first load transistor is identical to that of that of the second switching transistor.

5. The comparator as recited in claim 2, wherein the latching unit includes a first transistor and a second transistor having gates are cross-connected the main input terminal and the sub input terminal, respectively.

6. The comparator as recited in claim 1, wherein the

CMOS comparator includes a switching unit for switching to connect or disconnect between the latching unit in response to the clock signal.

7. The comparator as recited in claim 6, wherein the switching unit includes a third switching transistor and a fourth switching transistor having a gate receiving the clock signal, and forming a source-drain by connecting the main/sub terminals of the tracking/latching means and the latch means.